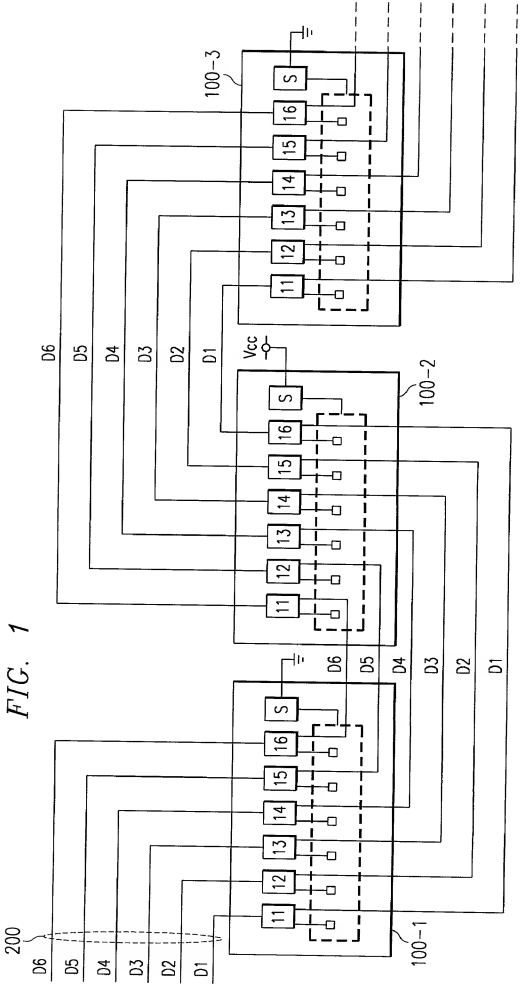


FIG. 1

FIG. 2

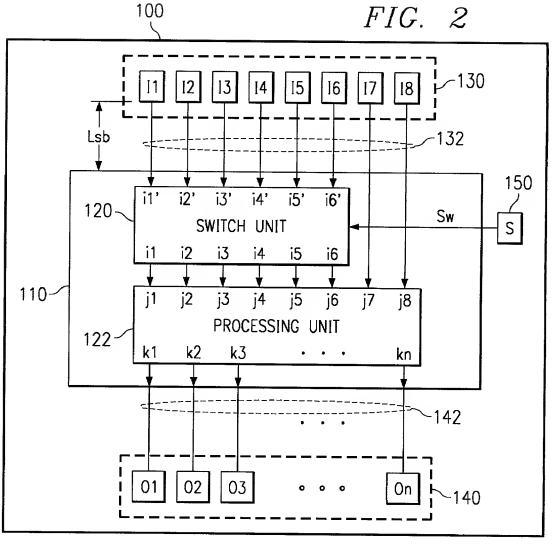
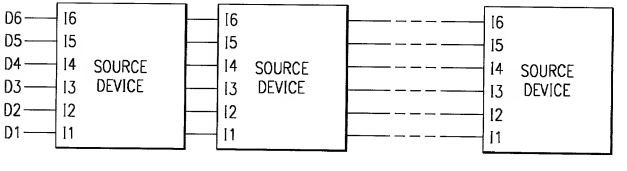


FIG. 3

Sw	INPUT	i1'	i2'	i3'	i4'	i5'	i6'
L	OUTPUT	i1	i2	i3	i4	i5	i6
H		i6	i5	i4	i3	i2	i1

FIG. 9



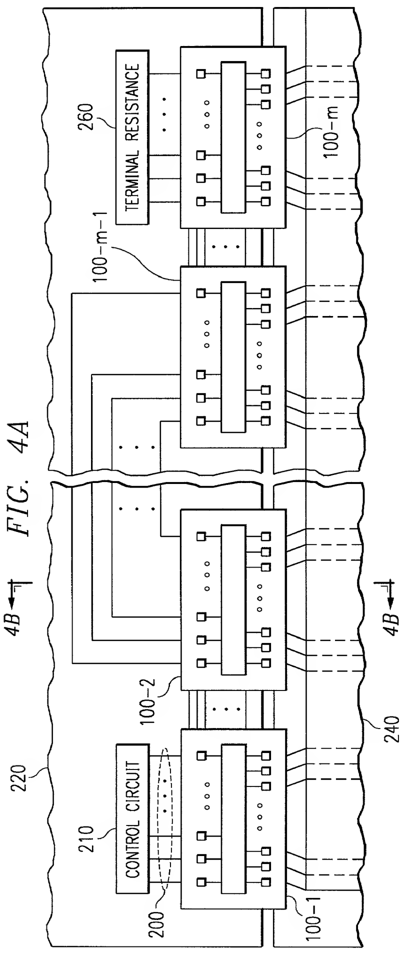

TERMINAL RESISTANCE
260
100-m
100-m-1
4B
4B
100-2
240
220
210
CONTROL CIRCUIT
200
100-1

FIG. 4A

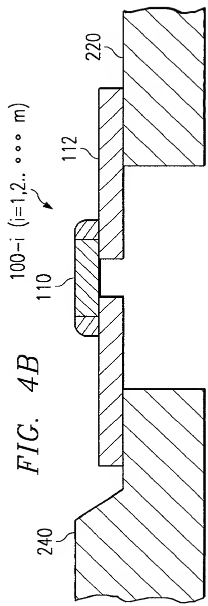

220
112
100-i (i=1,2,.. ∘∘∘ m)
110
240

FIG. 4B

FIG. 5

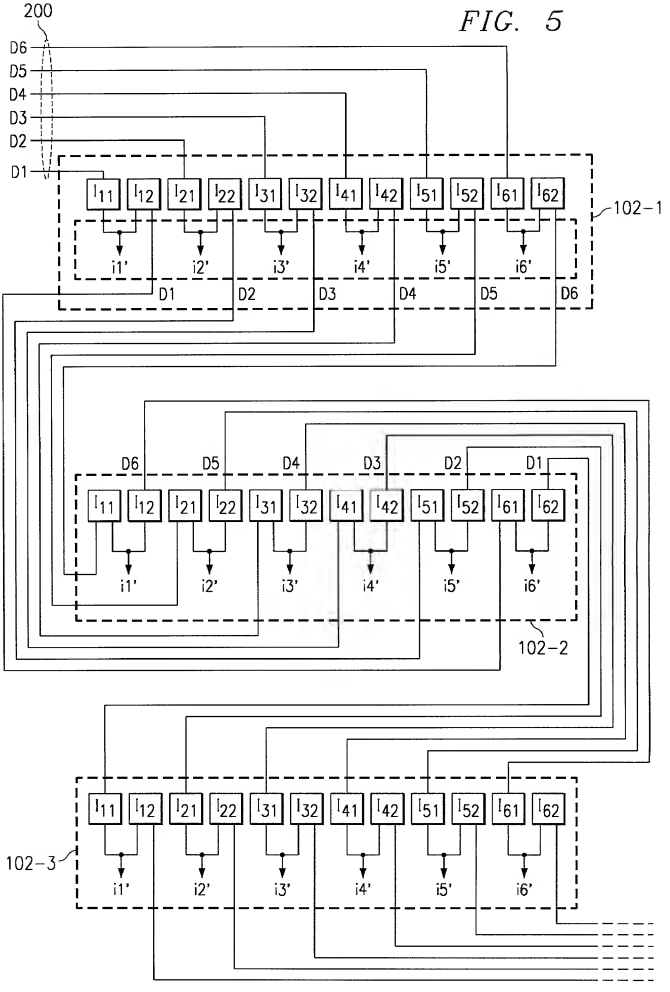
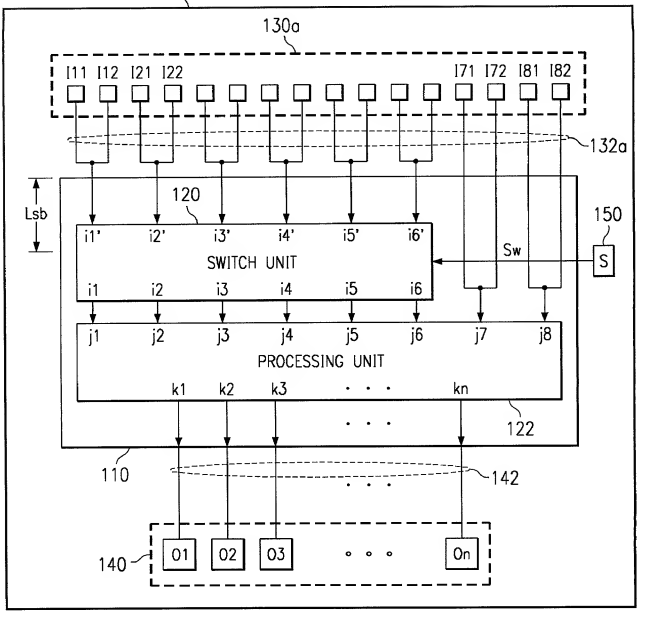

200
D6
D5
D4
D3
D2
D1
I11 I12 I21 I22 I31 I32 I41 I42 I51 I52 I61 I62
102-1
i1' i2' i3' i4' i5' i6'
D1 D2 D3 D4 D5 D6
D6 D5 D4 D3 D2 D1
I11 I12 I21 I22 I31 I32 I41 I42 I51 I52 I61 I62
i1' i2' i3' i4' i5' i6'
102-2
I11 I12 I21 I22 I31 I32 I41 I42 I51 I52 I61 I62
102-3
i1' i2' i3' i4' i5' i6'

FIG. 6


102
130a
I11 I12 I21 I22
I71 I72 I81 I82
132a
Lsb
120
150
i1' i2' i3' i4' i5' i6'
Sw
SWITCH UNIT
S
i1 i2 i3 i4 i5 i6
j1 j2 j3 j4 j5 j6 j7 j8
PROCESSING UNIT
k1 k2 k3 . . . kn
122
110
142
140
O1 O2 O3 . . . On

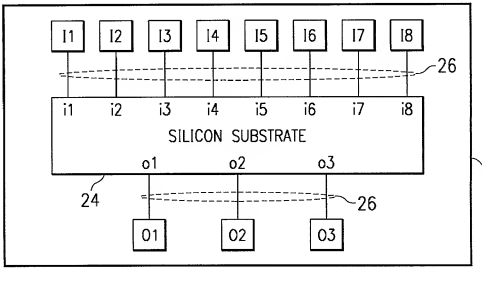

I1 I2 I3 I4 I5 I6 I7 I8
26
i1 i2 i3 i4 i5 i6 i7 i8
SILICON SUBSTRATE
o1 o2 o3
22
24
26
O1 O2 O3

FIG. 8

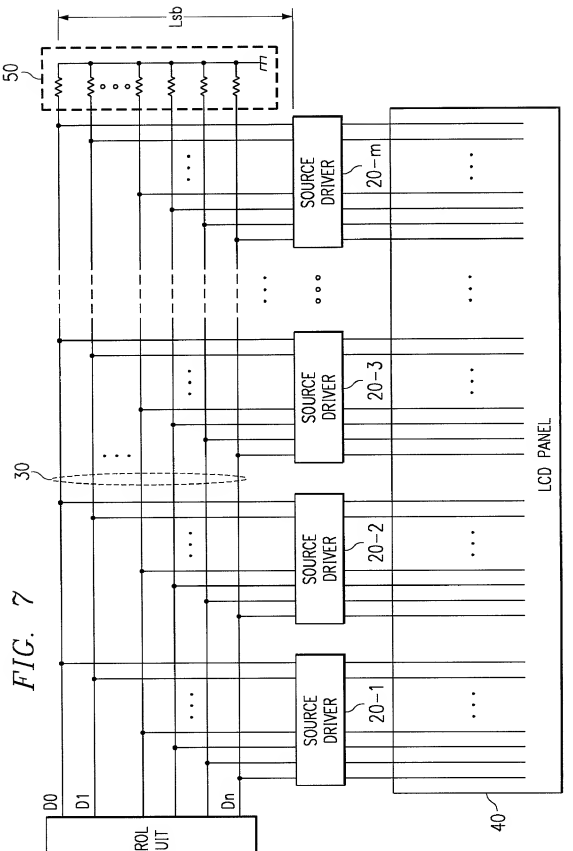

Lsb
50
m
30
10
CONTROL CIRCUIT
D0
D1
Dn
SOURCE DRIVER
20-1
20-2
20-3
20-m
LCD PANEL
40

FIG. 7